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10/650,325	08/27/2003	Jaime Bayan	NSC1P274/P05649	6886

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,325	BAYAN ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16,18-23,31-33 and 35-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16,18-23,31-33 and 35-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 14 is objected to because of the following informalities. Claim 14 recites a limitation of "by at least on of the lead segments" which should be by at least one of the lead segments. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites a unclear limitation of "... a plurality of electrical contacts arranged so that at least some of the contacts extend through the substrate having an exposed bottom surface on the bottom surface of the substrate ... " It is pointed out the instant invention does not disclose the arrangement of the electrical contacts defines the structure of some of the contacts. What is actually disclosed is that a center portion in Fig. 5B does not make an electrical contact since the center portion is a die pad while rest of the contacts working as an electrically conductive bump.

Claim 13 recites an unclear limitation of "a two dimensional microarray of rows and columns each comprised of at least one of the contacts and rows." It is confusing how the contacts arranged in columns and rows comprise one of the contacts and rows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-7, 9-12, 14-16, 18-20, 22-23, 31-33, 35-36 and 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang (US 6384472) in view of Lee (US 6713322).

Regarding claim 1, insofar as understood, Fig. 5 of Huang shows a substrate panel [Fig.10] for use in semiconductor packaging, comprising:

a lead-frame panel [602 in Fig. 10], including an array of device areas, each device area having a plurality of contacts exposed on a bottom surface of the substrate panel,

a plurality of wire bonding landings [106] exposed on a top surface of the substrate panel,

lead segments [104] that electrically couple selected wire bonding landings to associated electrical contacts [col. 4, lines 31-32]; and

a dielectric material [124] that fills spaces [122] between adjacent lead segments [col. 3, lines 54-56] wherein a top surface of the dielectric layer is substantially coplanar with the top surface of the substrate and the wire bonding landings, and a bottom surface of the dielectric layer is substantially coplanar with the bottom surface of the substrate panel and the electrical contacts thereby forming a substrate having substantially planar top and bottom surfaces.

Fig. 5 of Huang shows most aspect of the instant invention except "a plurality of electrical contacts arranged so that at least some of the contacts extend through the substrate having an exposed bottom surface on the bottom surface of the substrate." Fig. 8 of Lee shows

an lead frame configuration wherein the portion [6b] extending through the substrate (having the same thickness of the lead frame) with an exposed bottom, and the electrical contact is made (through a wire connection from the semiconductor device [20]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have a plurality of electrical contacts extending through the substrate to exposed bottom surface of the substrate for an condense electrical connection.

Regarding claim 3, Fig. 8 of Lee shows a semiconductor device wherein the wire bonding landings [10a, 10c] are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel and therefore, the dielectric material of the substrate is formed underneath the landing to give support to the wire bonding landings said support being sufficient to structurally reinforce the landings d-using a wire bond process.

Regarding claim 4, Fig. 5 of Huang shows at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

Regarding claim 5, Fig. 10 of Huang shows the device areas are arranged in at least one two dimensional array such that the substrate has at least two dimensional array of device area.

Regarding claim 6, Fig. 5 of Huang shows the most aspect of the instant invention except "the lead-frame further comprises a matrix of tie bars, the tie bars being positioned between immediately adjacent device areas in the two dimensional array of device areas and configured to support the lead segments." Fig. 11 of Lee shows a semiconductor device wherein the lead-frame [100] further comprises a matrix of tie bars [4], the tie bars being positioned between

adjacent device areas in the two dimensional array of device areas and configured to support the lead segments [col. 3, lines 34-37].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have a matrix of tie bars positioned between adjacent device areas in the two dimensional array of device areas and configured to support the lead segments for a secure package configuration.

Regarding claim 7, Fig. 5 of Huang shows each device area further includes a die attach pad [102], the die attach pad being exposed on the top surface of the substrate panel.

Regarding claim 9, it is obvious that at least one of the wire bonding landings is electrically coupled to the die attach pad by a lead segment since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

Regarding claim 10, Fig. 8 of Lee shows a semiconductor device wherein "at least one of the contacts [6] is located between the wire bonding landings [10] and the die attach pad [8].

Regarding claim 11, Fig. 5 of Huang shows a substrate panel [Fig. 10] for use in semiconductor packaging, comprising:

a lead-frame [602 in Fig. 10] panel including a two dimensional array of device areas, each device area having,

a plurality of contacts exposed on a bottom surface of the substrate panel a plurality of wire bonding landings [106] exposed on a top surface of the substrate panel, and

lead segments [104] configured to electrically couple selected wire bonding landings to associated contacts [col. 4, lines 31-32]; and

a dielectric material [124] that fills spaces [122] between adjacent lead segments and underlies at least a portion of each of the wire bonding landings, wherein a top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings, and a bottom surface of the dielectric material is substantially coplanar with the bottom surface of the substrate panel and the lead contacts; and

wherein at least some of the wire bonding landings are thinner than the substrate panel, such that the thinner wire bonding landings are not exposed on the bottom surface of the substrate panel, and at least selected portions of the lead segments are thinner than the substrate panel such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate panel.

Fig. 5 of Huang shows the most aspect of the instant invention except "the contacts are arranged in a microarray configuration." Fig. 4 of Lee shows a semiconductor device wherein the contacts are arranged in a microarray configuration.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the contacts arranged in a microarray configuration for a compact packaging.

Regarding claim 12, Fig. 5 of Huang shows each device area further includes a die attach pad [102], the die attach pad being exposed on the top surface of the substrate panel.

Regarding claim 14, it is inherent/obvious that at least one of the wire bonding landings is electrically coupled to the die attach pad by at least on of the lead segments since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

Regarding claim 15, Fig. 5 of Huang shows a packaged integrated circuit, comprising:

a substrate [600 in Fig. 10] including a plurality of contacts exposed on a bottom surface, a plurality of wire bonding landings [1-6] exposed on a top surface, lead segments[104] electrically coupling the wire bonding landings to associated lead contacts and a first dielectric layer [124] that fills spaces [122] between adjacent lead segments and fills space under the wire bond landings, wherein a top surface of the dielectric layer is substantially coplanar with the top surface of the substrate and the wire bonding landings, and a bottom surface of the dielectric layer is substantially coplanar with the bottom surface of the substrate panel and substantially coplanar with said contact surfaces thereby forming a substrate having substantially planar top and bottom surfaces;

a die [130] mounted on the substrate, the die having a plurality of bond pads configured for electrical connection [through wire 140] to the wire bonding landings;

a plurality of connectors for electrically connecting the plurality of bond pads to associated wire bonding landings [col. 4, lines 31-32]; and

a second dielectric layer [a transparent material in the space 126; col. 4, lines 61-63] that encapsulates the die and the plurality of connectors and covers at least a portion of the top surface of the substrate.

Fig. 5 of Huang shows the most aspect of the instant invention except "contacts configures for electrical contacts underneath the substrate." Fig. 11 of Lee shows a semiconductor device wherein contacts configures for electrical contacts [6b] underneath the substrate

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have contacts configured for electrical contacts underneath the substrate for a compact packaging.

Regarding claim 16, Fig. 5 of Huang shows the first (124 between the gaps) and second dielectric layers (126) are not integrally formed however, fails to show "the first and second dielectric layers are formed from substantially the same materials." Fig. 10 of Lee shows a semiconductor device wherein the first and second dielectric layers are formed from substantially the same materials [26; a sealing material]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the first and second dielectric layers formed from substantially the same materials to reduce the processing steps.

Regarding claim 18, Fig. 8 of Lee shows a semiconductor device wherein the wire bonding landings [10a, 10c] are thinner than the substrate panel, such that the wire bonding landings are not exposed on the bottom surface of the substrate panel

Regarding claim 19, Fig. 5 of Huang shows at least selected portions of the lead segments are thinner than the thickness of the lead-frame, such that the selected portions of the lead segments are not exposed on the bottom surface of the substrate.

Regarding claim 20, Fig. 8 of Lee shows a semiconductor device wherein a die attach pad [8] surrounded by the lead contacts [6].

Regarding claims 22, it is inherent/obvious that at least one of the wire bonding landings is directly electrically coupled (through the direct connection to the landing portion of the lead frame) to the die attach pad (through the direct connection to the landing portion of the lead

frame) by only an additional lead segment since Fig. 5 of Huang shows the wire bonding landings and the die pad are a portion of the same lead frame [100].

Regarding claim 23, Fig. 8 of Lee shows at least one of the contacts [6b] is located betweenthe wire landings and the die pad.

Regarding claim 31, Fig. 8 of Lee shows a semiconductor device wherein the wire bonding landings (the portion of the lead frame with a wire connection) are located radially further from a center of their associated device area than their associated contacts and wherein the substrate panel has substantially planar top and bottom surfaces with the wire bond landings and the lead segments being exposed on the top surface of the substrate not the bottom surface of the substrate.

Regarding claims 32 and 33, Fig. 9 of Lee shows at least some of the wire bonding landings have a width that is wider than an immediately adjacent portion of their associated lead segments and a thickness that is substantially the same as their associated lead segments, therefore the increased width of said wire bonding landings facilitates wire bonding to said landings.

Regarding claim 35, Fig. 5 of Huang shows the package is a lead frame based micro array package.

Regarding claim 36, Fig. 5 of Huang shows the most aspect of the instant invention except "the contacts are arranged in a microarray configuration." Fig. 4 of Lee shows a semiconductor device wherein the contacts are arranged in a microarray configuration.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the contacts arranged in a microarray configuration for a compact packaging.

Regarding claims 40 and 41, Fig. 5 of Huang shows a substrate panel wherein at least one of the wire bonding landings includes a support footing (a portion of the landing 106 below the molding 124) below that extends downward from the bottom surface of said wire bonding landings, each footing configured to support the landing during a wirebonding process and configured to have an exposed surface that is substantially coplanar with the bottom surface of the substrate panel.

Claims 8 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang and Lee as applied to claim 7 above, and further in view of Chien-Hung et al. (US Pat. Pub. 2003/006055), hereinafter Chien-Hung.

Regarding claim 8, the combined teachings of Huang and Lee show the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel." Fig. 1 of Chien-Hung shows a semiconductor wherein "the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate panel."

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Chien-Hung into the device of Huang and Lee in order to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate panel/a lead frame to improve the mounting capability to a circuit board.

Regarding claim 38, Fig. 8 of Lee shows the plurality of contacts and the plurality of posts exposed on the bottom surface of the substrate panel are arranged in a micro array.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang and Lee as applied to claim 12 above, and further in view of Chien-Hung.

Regarding claim 13, insofar as understood, Fig. 5 of Huang shows the most aspect of the instant invention except "the contacts surround the die attach pad, and wherein the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the contacts and the posts being arranged in a two dimensional array." Fig. 8 of Lee shows a semiconductor device wherein the contacts [6] surround the die attach pad [8] while arranged in a two dimensional array.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Lee into the device of Huang in order to have the contacts located between the wire bonding landings and arranged in a two dimensional array to form a ground contact as taught by Lee.

The combined teachings of Huang and Lee shows the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate panel, the posts being arranged in a two dimensional array." Fig. 1 of Chien-Hung shows a semiconductor wherein the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate panel and arranged in a two dimensional array.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Chien-Hung into the device of Huang and Lee in order

to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate panel [a lead frame] and arranged in a two dimensional array to improve the mounting capability to a circuit board.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang and Lee as applied to claim 20 above, and further in view of Chien-Hung.

Regarding claim 21, the combined teachings of Huang and Lee show the most aspect of the instant invention except "the die attach pad has a plurality of posts exposed on the bottom surface of the substrate." Fig. 1 of Chien-Hung shows a semiconductor wherein the die attach pad [130] has a plurality of posts [132] exposed on the bottom surface of the substrate/a lead frame.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Chien-Huang into the device of Huang and Lee in order to have the die attach pad with a plurality of posts exposed on the bottom surface of the substrate/a lead frame to improve the mounting capability to a circuit board.

Claims 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang and Lee as applied to claim 36 above, and further in view of Murtuza et al. (US 6849944), hereinafter Murtuza.

Regarding claim 37, the combined teachings of Huang and Lee show the most aspect of the instant invention except "the plurality of contacts arranged as a microarray are patterned in a

ball grid array (BOA) configuration." Fig. 2 of Murtuza shows a semiconductor with the plurality of contacts arranged in a ball grid array (BOA) configuration.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Murtuza into the device of Huang and Lee in order to have the plurality of contacts patterned in a ball grid array configuration to improve an underfill.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Huang, Lee and Chien-Hung as applied to claim 38 above, and further in view of Murtuza.

Regarding claim 39, the combined teachings of Huang, Lee and Murtuza show the most aspect of the instant invention except the contacts and posts on the bottom surface of the substrate panel are arranged in a BOA pattern." Fig. 2 of Murtuza shows a semiconductor with the plurality of contacts arranged in a ball grid array (BOA) configuration.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Murtuza into the device of Huang, Lee and Chien-Huang in order to have the plurality of contacts patterned in a ball grid array configuration to improve an underfill.

Response to Arguments

Applicant's arguments filed September 8, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims.

In addition, Examiner presents the remarks below in response to Applicant's arguments.

The Applicant's argument on the rejection under 35 U.S.C. 112 does not appear to be convincing. Applicant does not provide any factual support either with prior art or knowledge known to one skilled in the art. Furthermore, the instant invention explicitly discloses that a final product is encapsulated. See paragraph [0020], in particular [0021]. However, the rejection under 35 U.S.C. 112 is withdrawn assuming that the instant invention recites an intermediate product.

It is pointed out that the instant invention does not disclose "contacts ... arranged in a microarray configuration." The instant invention discloses that micro-array configuration of the devices on the lead frame panel.

Applicant further argues that "Huang also does not teach a 'top surface of the dielectric material is substantially coplanar with the top surface of the substrate panel and the wire bonding landings'. " It is pointed out that the instant invention recites that "a dielectric layer that fills spaces between the adjacent lead segment." And Huang show that the dielectric material between the lead segment is coplanar with the top surface of the substrate panel and the wire bonding landings. Note that the molding layer 124 of Huang is not a dielectric layer between the lead segment.

Applicant further argues that a tie bar in the Lee's reference does not meet the claim limitation. It is pointed out that Figures of the instant invention do not disclose tie bar in the embodiment of the instant invention. The instant invention discloses that prior art has the tie bars which is shown within the device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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